CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

a die attach surface having a first pedestal;

a first semiconductor die having a first surface formed with a first cavity for mounting the first semiconductor die on the first pedestal; and

a reactive component disposed on a second surface of the first semiconductor die in a region overlying the first pedestal.

2. The semiconductor device of claim 1, where the reactive component includes an inductor.

3. A semiconductor device, comprising:

a first semiconductor die having a first surface formed with a first cavity; and

a base; and

a first pedestal formed on the base for engaging with the cavity, where the first pedestal has a recessed region for forming a dielectric volume.

4. The semiconductor device of claim 3, further comprising an electrical component disposed on a second surface of the semiconductor die in a region overlying the dielectric volume.

5. The semiconductor device of claim 4, where the electrical component operates as an inductor.

6. The semiconductor device of claim 3, where the dielectric volume comprises a dielectric material.

7. The semiconductor device of claim 6, where the dielectric material is gaseous.

8. The semiconductor device of claim 3, where a surface of the pedestal includes a conductive material for operating as a ground shield of the first semiconductor die.

9. The semiconductor device of claim 3, further comprising:

a second pedestal disposed on the base; and

a second semiconductor die having a first surface formed with a cavity for mounting to the second pedestal.

10. The semiconductor device of claim 9, further comprising a dielectric material disposed between the first semiconductor die and the second semiconductor die.

11. The semiconductor device of claim 9, further comprising a conductor disposed for coupling an electrical signal between the first semiconductor die and the second semiconductor die.

12. A method of operating a semiconductor device, comprising the steps of:

providing a base having a first pedestal for mounting against a first cavity of a first semiconductor die; and

generating a first field with a first electrical component of the semiconductor die, where the first field penetrates a recessed region of the first pedestal.

13. The method of claim 12, where the step of generating includes the step of inducing a magnetic field in the recessed region.

14. The method of claim 12, where the step of generating includes the step of generating the first field in a dielectric material of the recessed region.

15. The method of claim 12, further comprising the steps of:

generating a second field with a second electrical component of the semiconductor die; and

terminating the second electric field on a conductive portion of the pedestal.

16. The method of claim 12, further comprising the steps of:

providing a second pedestal of the base for mounting against a second cavity of a second semiconductor die; and

coupling an electrical signal from the first semiconductor die to the second semiconductor die.

17. An integrated circuit, comprising:

a semiconductor die having a first surface formed with a recession; and

a die attach base having a raised appurtenance for aligning with the recession of the semiconductor die; and

an inductor formed on a second surface of the semiconductor die to overlie a recessed region of the raised appurtenance.

18. A die attach mount comprising;

a base; and

a die attach pedestal configured to engage with a first semiconductor die, where the die attach pedestal has a recessed region for forming a dielectric volume, and the first semiconductor die having a first surface formed with a first cavity configured to engage with the die attach pedestal.

19. The die attach mount of claim 18, wherein the die attach pedestal comprises a bilaterally symmetrical trapezoidal cross-section and wherein the smallest angles in the cross-section are about 54.73 degrees.

20. The die attach mount of claim 18, wherein the base and the pedestal comprise:

a generally planar dielectric material forming the base; and

a frustum of a four-sided pyramid having a broad base coupled to the base.

21. The die attach mount of claim 18, wherein the base and the pedestal comprise:

a generally planar dielectric material forming the base;

a frustum of a four-sided pyramid having a broad base coupled to the base, a height of the frustum being configured to be slightly less than a depth of a cavity formed in a rear surface of the semiconductor die.

22. The die attach mount of claim 18, wherein the base and the pedestal comprise:

a generally planar dielectric material forming the base;

a frustum of a four-sided pyramid forming the pedestal, the pedestal having a broad base coupled to the base; and

a conductive coating formed over some exposed surfaces of the base and the pedestal, wherein no conductive coating is present on regions of the pedestal configured to be placed in proximity to one or more dielectric platforms formed on the first semiconductor die, the dielectric platform having a lower surface extending into the first cavity.

23. The die attach mount of claim 18, wherein the base and the pedestal comprise conductive material.

24. The die attach mount of claim 18, wherein the base and the pedestal comprise:

a generally planar base;

a frustum of a four-sided pyramid formed from conductive material and having a broad base coupled a surface of the generally planar base, a height of the frustum being configured to be slightly less than a depth of a cavity formed in a rear surface of the semiconductor die, the frustum further comprising a small cavity formed on a top surface of the pedestal on regions of the pedestal configured to be placed in proximity to one or more dielectric platforms formed on the first semiconductor die.

25. The die attach mount of claim 18, further comprising a first semiconductor die having a first surface defining a recessed region wherein the pedestal is electrically and mechanically engaged with at least a portion of the recessed region.

26. The die attach mount of claim 18, further comprising a first semiconductor die having a first surface defining a recessed region wherein the pedestal is mechanically engaged with at least a portion of the recessed region.